UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,811	02/20/2004	Masatoshi Takami	042123	3939

38834 7590 02/24/2005

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,811	MASATOSHI TAKAMI	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-15* is/are rejected.

7)☒ Claim(s) *1-3,5,7,9 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-15) in the reply filed on 12/10/04 is acknowledged.

Claim Objections

2. Claims 1, 2, 5, 7, 9 and 13 are objected to because of the following informalities:

- Claim 1 lines 9-11 recites "a region where the region for the gate electrode formed in and the device region overlap each other." This wording is cumbersome and confusing. It is suggested that the limitation be amended to read "a region where the gate electrode and device region overlap each other" so as to clarify that which is applicants invention.
- Claim 2 lines 15-17 and 22-24 recites similar limitations as claim 1 pointed out above. These limitations should also be amended to clarify that which is applicant invention.
- Claim 5 line 3 recites "the metal layer," this should be corrected to recite either the **first** or **second** metal layer to correspond with claim 2, from which claim 5 depends.
- Claim 7 line 3 recites "the metal layer," this should be corrected to recite either the **first** or **second** metal layer to correspond with claim 2, from which claim 7 depends.

- Claim 9 recites "the metal layer" in lines 4 and 7, "the gate electrode" in line 5, and "the device region" in line 6, these should be corrected to recite either the **first** or **second** metal layer, gate electrode and device region to correspond with claim 2, from which claim 9 depends.
- Claim 11 line 3 recites "the metal layer," this should be corrected to recite either the **first** or **second** metal layer to correspond with claim 2, from which claim 11 depends.
- Claim 13 lines 4-5 recites "the metal layer," this should be corrected to recite either the **first** or **second** metal layer to correspond with claim 2, from which claim 13 depends.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 and 9 both recite limitations dealing with a ratio. The claims a gap between the semiconductor substrate and the metal layer, this gap presumably being a vertical measurement, as the first part of the ratio. However, the second "gap" in the ratio is indefinite as one cannot ascertain what gap is being claimed. It is indefinite as

to what gap is being claimed by "a gap between a region where the region for the gate electrode formed in and the device region overlap each other and the peripheral part of the metal layer." In reading this claim language without referring back to the specification to read definite limitations into this claim, one cannot determine what the claimed gap is or where one would measure it. Further, it is not clear as to whether "**a** region where the region for the gate electrode formed in" is claiming the same region as in claim 1 lines 9-11 or whether a different "region" is being defined. It is noted that he term "region" is a broad term itself as it can be interpreted to be a variety of sections or segments of a device.

5. Insofar as definite, and as best understood, the claims are rejected over prior art as follows. With regard to claims 8 and 9, since one cannot reasonably ascertain what ratio of gaps is actually being claimed, the ratio will be provisionally interpreted consistent with the ratio described on page 12 lines 14-17.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 6, 8, 10, 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by JP-09252131-A (cited on IDS submitted 3/29/04).

With regard to claim 1, JP-09252131-A discloses in figures 1-17 a semiconductor device comprising:

- a semiconductor substrate 10 having a device region (figure 5; the region encompassed by reference letter "T" is considered the device region);
- a transistor including a gate electrode G formed in the device region with a gate insulation film formed therebetween (figure 1 shows gate "G" labeled; though not labeled, the transistor has a gate dielectric as it is disclosed in the abstract as being a MOS transistor; MOS stands for "metal oxide semiconductor" and necessarily has a gate insulation film (oxide) formed under the gate); and
- a metal layer 16Q formed over the gate electrode with an insulation film 14 formed therebetween (figure 5), formed of a metal material having the property of occluding hydrogen and having a peripheral part 16C positioned outer of a region where the region for the gate electrode formed in and the device region overlap each other (figure 10 shows the composition of metal layer 16; the metal layer is formed of Titanium which occludes hydrogen; figure 5 shown the position of peripheral part 16C).

With regard to claim 6, as seen in figures 7 and 11, the metal layer 16Q is not connected to any other conductive layers and thus the potential of the metal layer 16Q is floating.

With regard to claim 8, the ratio of the gap (measured vertically) between the metal layer 16Q and the substrate to the gap (measured horizontally) between the gate electrode and the peripheral part of the metal layer is 0.32 or less than 0.32. Though

measurements are not shown for the gaps in the ratio, the structure as shown meets the claimed ratio. Further, with the broad "region" language of the claim, one can measure from the right side of the gate to the edge of peripheral portion 16C such that the ratio is roughly 1:4, which is less than 0.32.

With regard to claim 10, the metal layer of JP-09252131-A is disclosed in figure 10 as being formed of the metal material having the property of occluding hydrogen (Ti), and another metal film of a metal material which does not have the property of occluding hydrogen (Al).

With regard to claim 12, JP-09252131-A further disclose an interconnection layer 16S or 16D formed on the insulation film 14 and formed of the same metal film forming the metal layer 16Q.

With regard to claim 14, the metal material is titanium, magnesium, an alloy containing titanium or an alloy containing magnesium (Ti or TiN as shown in figure 10).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 7, 9, 11, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-09252131-A as applied to claims 1, 6, 8, 10, 12 and 14 above, and further in view of Lockwood (U.S. Patent No. 3,996,482).

Claim 2 recites a device having a first and second transistor, each transistor with the same limitations as the transistor in the device of claim 1. JP-09252131-A teaches a single transistor with all the claimed limitations of each individual transistor as shown above with regards to claim 1, however, JP-09252131-A does not teach two transistors in a single semiconductor device. It is well known in the semiconductor art to form multiple transistors together so that they may be interconnected into various circuit or arrays.

Lockwood teaches a circuit in figure 1 that includes multiple transistors 18/20/30/32/50/52/70 formed together using MOS LSI (large scale integration) techniques. Lockwood shows an advantage use for the transistor of JP-09252131-A in that it may be used in a current mirror circuit, inverter circuit, or bias network to produce a one shot multivibrator circuit.

JP-09252131-A and Lockwood are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a circuit such as Lockwood's using the transistor of JP-09252131-A. The motivation for doing so is to form an improved one shot multivibrator circuit where the period of its output pulse is independent of the threshold voltages of the transistors used in the circuit design. Therefore, it would have been obvious to combine JP-09252131-A with Lockwood to obtain the invention of claim 2.

With regard to claim 7, as seen in figures 7 and 11 of JP-09252131-A, the metal layer 16Q is not connected to any other conductive layers and thus the potential of the metal layer 16Q is floating.

With regard to claim 9, the ratio of the gap (measured vertically) between the metal layer 16Q and the substrate to the gap (measured horizontally) between the gate electrode and the peripheral part of the metal layer is 0.32 or less than 0.32. Though measurements are not shown for the gaps in the ratio, the structure as shown meets the claimed ratio. Further, with the broad "region" language of the claim, one can measure from the right side of the gate to the edge of peripheral portion 16C such that the ratio is roughly 1:4, which is less than 0.32.

With regard to claim 11, the metal layer of JP-09252131-A is taught in figure 10 as being formed of the metal material having the property of occluding hydrogen (Ti), and another metal film of a metal material which does not have the property of occluding hydrogen (Al).

With regard to claim 13, JP-09252131-A further teach an interconnection layer 16S or 16D formed on the insulation film 14 and formed of the same metal film forming the metal layer 16Q.

With regard to claim 15, in combining the references, the transistor of JP-09252131-A is used in the circuit shown in Lockwood figure 1, thus the transistor forms a part of a current mirror circuit.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP-09252131-A as applied to claims 1, 6, 8, 10, 12 and 14 above, and further in view of Dixit et al. (US 2002/0185664 A1).

JP-09252131-A does not teach the potential of the metal layer being fixed to a prescribed potential. The metal layer 16Q of JP-09252131-A is formed on the first level of metallization along with the source/drain contacts 16S/16D but is not connected to any other conductive structures and is in fact a dummy layer in that it does not contribute to device operation.

Dixit et al. teach metallization layers in a large scale integrated circuit. Dixit et al. teach that dummy layers are included in circuits but have previously been left floating (Dixit et al., paragraphs 0007-0008). Dixit et al. teach connecting dummy metal to ground.

JP-09252131-A and Dixit et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the metal layer 16Q of JP-09252131-A such that it's potential is fixed to a prescribed potential of ground. The motivation for doing so is to avoid unwanted cross-talk or noise in the chip. Therefore, it would have been obvious to combine JP-09252131-A with Dixit et al. to obtain the invention of claim 4.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP-09252131-A in view of Lockwood (U.S. Patent No. 3,996,482) as applied to claims 2, 7, 9, 11, 13 and 15 above, and further in view of Dixit et al. (US 2002/0185664 A1).

JP-09252131-A with Lockwood do not teach the potential of the metal layer being fixed to a prescribed potential. The metal layer 16Q of JP-09252131-A is formed on the first level of metallization along with the source/drain contacts 16S/16D but is not

connected to any other conductive structures and is in fact a dummy layer in that it does not contribute to device operation.

Dixit et al. teach metallization layers in a large scale integrated circuit. Dixit et al. teach that dummy layers are included in circuits but have previously been left floating (Dixit et al., paragraphs 0007-0008). Dixit et al. teach connecting dummy metal to ground.

JP-09252131-A with Lockwood and Dixit et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the metal layer 16Q of JP-09252131-A such that it's potential is fixed to a prescribed potential of ground. The motivation for doing so is to avoid unwanted cross-talk or noise in the chip. Therefore, it would have been obvious to combine JP-09252131-A and Lockwood with Dixit et al. to obtain the invention of claim 5.

Allowable Subject Matter

12. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: Prior art of record fails to teach, disclose, or suggest, either alone or in combination, the combination of limitations as claimed in claim 3 where the first and

second metal layer which occluded hydrogen are overlapping the first and second gate electrode and the first and second metal layer are electrically connected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N. Drew Richards
AU 2815